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Enhancing the Electrical Properties of a Flexible Transparent Graphene-Based Field-Effect Transistor Using Electropolished Copper Foil for Graphene Growth

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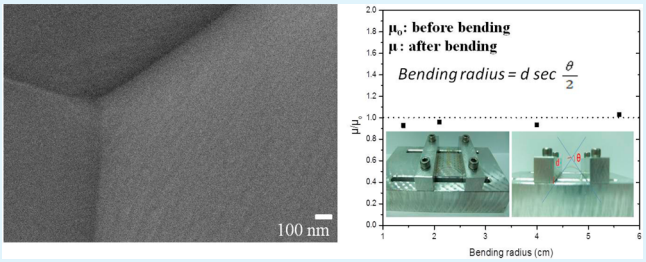
Supporting Information

ABSTRACT: Flexible transparent graphene-based field-effect transistors (Gr-FETs) were fabricated using large-area single-layer graphene synthesized through low-pressure chemical vapor deposition on a pretreated copper (Cu) foil, followed by transfer of the graphene from the Cu foil to a poly(ethylene terephthalate) (PET) substrate. The electropolishing method was adopted to smooth the surface of the Cu foil, which is a crucial factor because it affects the defect density of graphene films on the PET substrate after transfer and the electronic transport property of the graphene-based devices. The influence of the electropolishing process on the graphene properties was examined using a Raman spectroscope, a scanning electron microscope, and an optical microscope. When the electropolishing process was adopted to improve the graphene quality, the carrier mobility of the flexible transparent Gr-FETs was enhanced from 90 to 340 $cm^2/(V\ s)$. Furthermore, variation of the carrier mobility was lower than 10% when the bending radius of the flexible device was decreased from 6.0 to 1.0 cm.



KEYWORDS: *graphene, field-effect transistors, flexible, transparent, electropolishing*

1. INTRODUCTION

Single-layer graphene with a regular hexagonal two-dimensional (2D) structure possessing high chemical stability, superior mechanical properties, extremely high carrier density, and outstanding optical transparency has numerous promising applications, which has generated substantial interest in the electronic and nanotechnology communities.[1−5] Among the potential applications, graphene-based field-effect transistors (Gr-FETs) attracted the most scientific attention because graphene possesses high carrier mobility of up to 2×10^5 $cm^2/(V\ s)$, which is higher than that of silicon (Si) by over 2 orders of magnitude.[6] Furthermore, at low carrier density, suspended graphene exhibits near-ballistic behavior, which can potentially be used to fabricate smaller and higher-speed transistors compared with Si-based FETs and could thus replace Si chips and initiate a revolution in consumer electronic products.[7]

Two primary methods currently exist for synthesizing graphene: bottom-up and top-down. The bottom-up methods include chemical vapor deposition (CVD), epitaxial growth, and solvothermal, whereas the top-down methods include micromechanical cleavage, chemical synthesis through the oxidation of graphite, thermal exfoliation and reduction, and electrolytic exfoliation.[8−13] Considering the compatibility of graphene with the present semiconductor processes for fabricating Gr-FETs, growing large-area, high-quality, and defect-free graphene is imperative. Among the proposed methods for synthesizing single- or double-layer graphene, adopting the CVD method and using copper (Cu) foil as the substrate seems to be the most promising method for preparing high-quality graphene.[14−19]

When CVD was adopted for growing graphene on Cu foil, the graphene conformed to the Cu surface, indicating that the presence of defects, hills, or valleys on the uneven Cu foil generated nucleation sites for graphene deposition, consequently forming graphene with numerous foldings. The roughness of unpolished Cu foil ranges from 300 to 400 nm, which is substantially greater than that of single-layer graphene (less than 1.0 nm in thickness). The quality of single-layer graphene is affected by the flatness of the as-received Cu foil during the growing and transferring processes. Therefore, using highly even Cu foil for graphene deposition is essential for fabricating a high-performance Gr-FET.[23−25]

This study involved fabricating flexible transparent Gr-FETs by depositing graphene onto Cu foil and subsequently transferring the as-synthesized graphene onto a poly(ethylene terephthalate) (PET) substrate. Flexible transparent Gr-FETs have numerous potential applications, such as use in flexible electronics, disposable sensors, and wearable solar cells.[20−22] We also used the electropolishing method to smooth the Cu foil that was subsequently adopted for graphene deposition by using CVD. The Cu foils, with and without being subjected to electropolishing, were designed as up-Cu and p-Cu foils,

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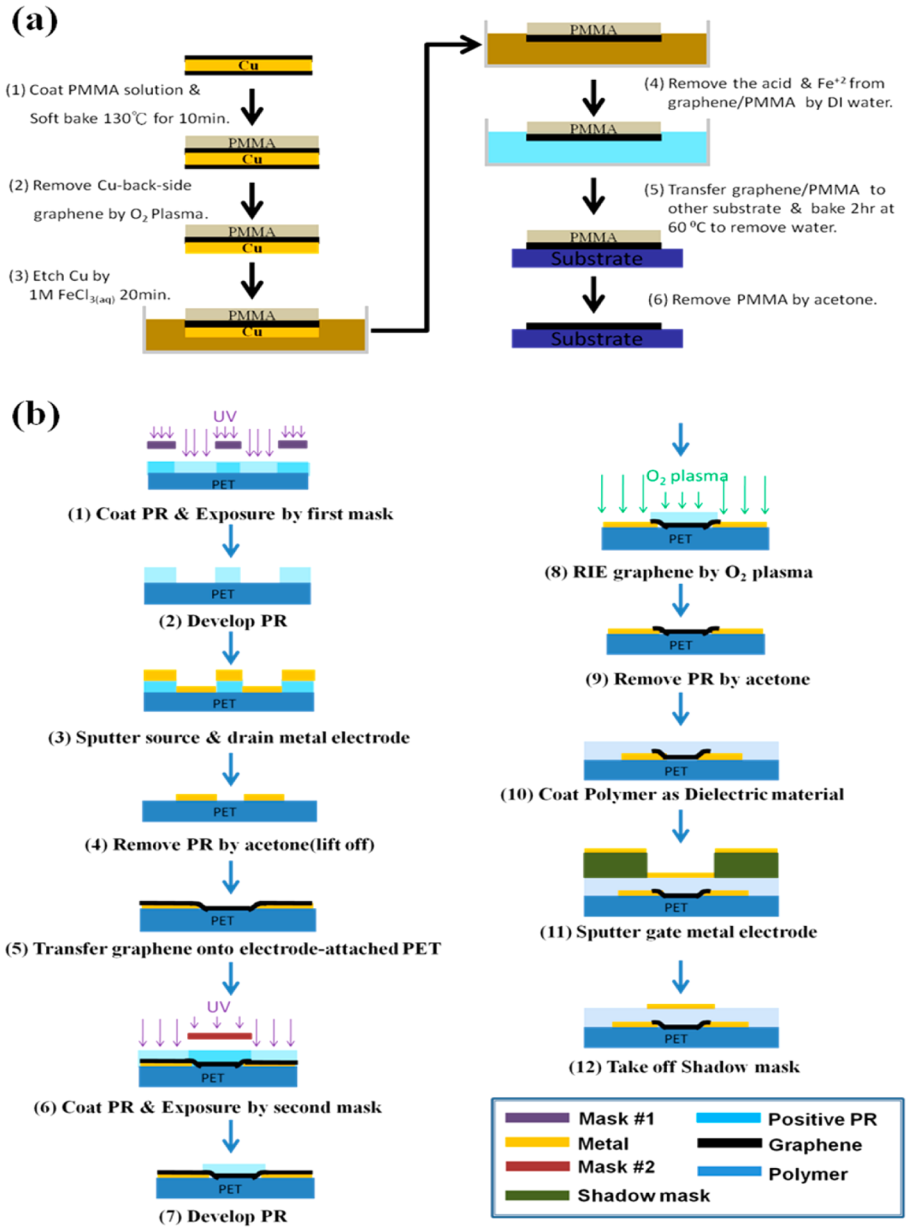

Figure 1. (a) Flowchart of the transferring process. (b) Flowchart of the preparation process for flexible transparent Gr-FETs.

respectively. The quality of the synthesized graphene was examined using Raman spectroscopy, atomic force microscopy (AFM), optical microscopy (OM), and scanning electron microscopy (SEM). The Raman spectrum intensity, AFM topography, and SEM images of graphene prepared using the up-Cu and p-Cu foils were compared, and their possible mechanisms are discussed. Fabrications of top-gate Gr-FETs on transparent PET film were achieved using the photolithography process, and their electronic properties were measured. The carrier mobility of the Gr-FETs, based on graphene prepared using the p-Cu foil, was substantially higher than that of the Gr-FETs prepared using the up-Cu foil. The current−voltage relationships of the Gr-FETs were measured, and the results were discussed.

2. EXPERIMENTAL SECTION

2.1. Preparation of Cu Foil with High Flatness. A Cu foil and a Cu plate were adopted as an anode and a cathode, respectively, which were immersed in electrolyte composed of 85% phosphoric acid (containing 1.0 mL of glycerol and 2.2 mL of glacial acetic acid). The electropolishing treatments were performed at a voltage of 1.5 V for 20 min.

2.2. CVD Growth Process. A Cu substrate (No. 13382, Alfa Aesar Inc.) that was 99.98% pure and 25 μm thick was employed in this study. To remove copper oxide from the Cu foil, the Cu foil was immersed in 1.0 M CH_3COOH for 30 min and subsequently diluted with deionized (DI) water, followed a drying process by nitrogen gun. The Cu foil was subsequently placed in a tube furnace and annealed at 800 °C for 30 min at 36.5 Torr under flow conditions containing argon and hydrogen with flow rates of 200 and 100 sccm, respectively. During the annealing treatment, the residual copper oxide was removed and the Cu crystalline size was increased, consequently alleviating the influence of the Cu grain boundary on the quality of the synthesized graphene. All the efforts were used to reduce the roughness of the Cu surface. In the graphene deposition process, we used CH_4 as a precursor, which was channeled into the furnace and pyrolyzed at 1000 °C for 10 min. Finally, the furnace temperature was

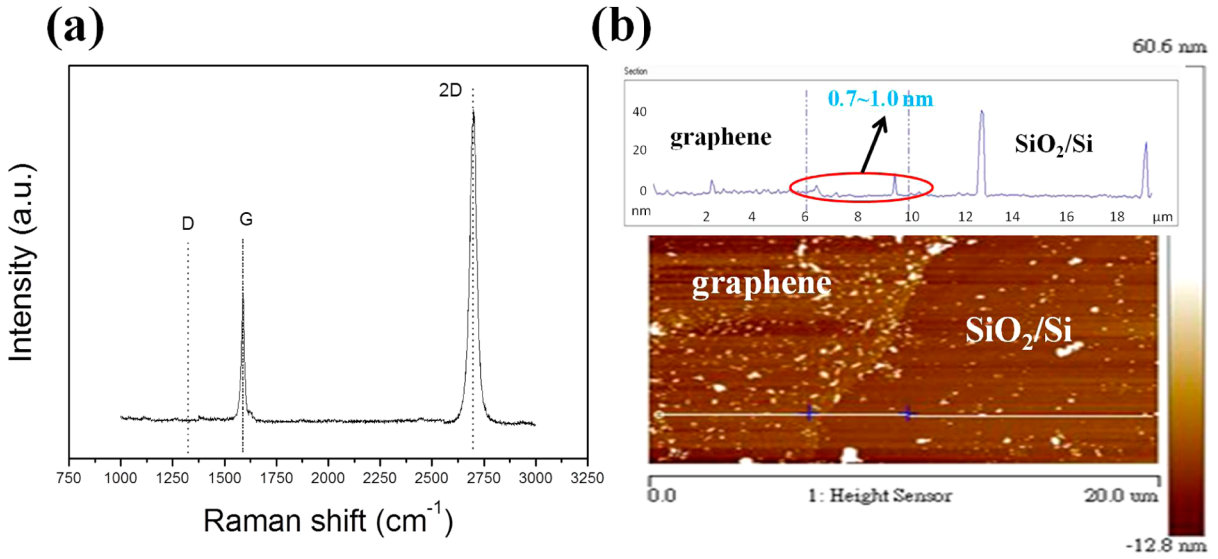

Figure 2. (a) Raman spectrum of graphene on p-Cu foil. (b) AFM images of graphene transferred from the p-Cu foil to the SiO_2/Si substrate.

cooled from 1000 to 700 °C at a cooling rate of 15 °C/min, followed by a rapid cooling process to room temperature.

2.3. Transfer Process. Figure 1a illustrates the transfer process. Poly(methyl methacrylate) (PMMA; 950000 MW, 6 wt % in anisole) was spin-coated onto one side of the graphene-deposited Cu foil, whereas the graphene on the other side of the Cu foil was removed using O_2 plasma. The Cu foil in the PMMA/graphene/Cu foil sandwich layer was etched using an etchant of 1.0 M $FeCl_3$. Subsequently, graphene/PMMA was placed in DI water to rinse the residue etchant. Graphene/PMMA was then transferred to the PET substrate to form a PMMA/graphene/PET structure. Graphene on the PET substrate was obtained by baking the PMMA/graphene/PET film at 60 °C for 1−2 h, followed by immersing the dry film in acetone to remove PMMA.

2.4. Fabrication of Flexible Transparent Gr-FET. We selected PET with a thickness of 125 μm as a transparent substrate, as shown in Figure 1b. The fabrication steps included (1) coating the photoresist (PR) on PET and exposing the PR by using the first mask, (2) developing the PR, (3) sputtering the source and drain, (4) removing the PR, (5) transferring graphene to the electrode-coated PET, (6) coating the PR and exposing it by using the second mask, (7) developing the PR, (8) reactive-ion etching graphene by using O_2 plasma, (9) removing the PR, (10) coating PMMA on graphene and electrodes as a dielectric layer, (11) sputtering the gate electrode by using a shadow mask, and (12) removing the shadow mask. The source and drain electrodes (titanium/gold, 30 nm/60 nm) were formed by using photolithography and a lift-off process (steps 1−4). After graphene was transferred to the plastic substrate, the patterns of graphene were formed using the secondary photolithography process and O_2 plasma etching (steps 6−8). Graphene could, therefore, successfully make contact with the source and drain electrodes. At step 10, the PMMA solution was spun onto the PET substrate followed by a baking process conducted at 130 °C for 10 min. The PMMA film served as a dielectric layer. The top-gate Gr-FETs were obtained after the top-gate electrode (gold, 100 nm) was sputtered through a shadow mask (steps 11 and 12).

2.5. Characterization and Electrical Measurement. The thickness and roughness of the graphene were measured using AFM. The morphologies of graphene grown on the up-Cu and p-Cu foils were examined using SEM, and the quality of the transferred graphene on the SiO_2/Si and PET substrates was determined using Raman spectroscopy and OM. Ultraviolet/visible spectroscopy was adopted for measuring the transmittance of graphene, and the electrical properties of the Gr-FETs were characterized using a semiconductor parameter analyzer (4200-SCS semiconductor parameter analyzer, Keithley). The carrier mobility (μ_{FE}) was calculated according to eq 1

$$\mu_{FE} = \frac{L_{ch}}{W_{ch}V_{DS}}\frac{t_{ox}}{k_{ox}\varepsilon_o}\frac{dI_D}{dV_{GS}} \quad (1)$$

where L_{ch} and W_{ch} are the channel length and width, respectively, t_{ox} and k_{ox} are the thickness and dielectric coefficient of the gate dielectric, respectively, ε_0 is the permittivity of free space, V_{DS} is the applied voltage between the drain and source, I_D is the drain current, and V_{GS} is the applied voltage on the gate. Bending tests were conducted on the Gr-FETs by using a homemade device, and variations on the carrier mobility of the Gr-FETs with and without bending were measured.

3. RESULTS AND DISCUSSION

High-quality single-layer graphene was synthesized on p-Cu foil by using low-pressure thermal CVD. Three characteristic peaks at 1250−1350 cm^{-1} (D-band), 1580−1600 cm^{-1} (G-band), and 2650−2700 cm^{-1} (2D-band) in the Raman spectrum were detected. The D-band indicates defects in the graphene structure or the presence of amorphous graphite. The G-band represents the E_{2g} vibration mode of sp^2-bonded carbon, and the 2D-band refers to a second-order two-phonon process. The position and shape of the 2D peak as well as the intensity ratio of the 2D-band and G-band (I_{2D}/I_G) are typically used for determining the number of graphene layers.[26−29] Features of the graphitic structure increased as the number of graphene layer increased, which weakened the 2D-band intensity; therefore, the I_{2D}/I_G ratio is a suitable index for determining the presence of single-layer graphene. A criterion of I_{2D}/I_G greater than 2.0 indicates the presence of single-layer graphene. The Raman spectrum of the as-synthesized graphene, using the p-Cu foil as a substrate, is shown in Figure 2a. A low insignificant D-band intensity incorporated with a high I_{2D}/I_G ratio greater than 2.0 indicates the synthesis of high-quality single-layer graphene.

The thickness of the as-synthesized graphene was determined using AFM by measuring the height of the graphene transferred from the p-Cu foil to the SiO_2/Si substrate. As shown in Figure 2b, an obvious border existed between the SiO_2/Si substrate (left) and graphene (right). AFM involving a tapping mode was applied for measuring the graphene thickness by scanning the surface with a size of 20 × 20 μm^2. The thickness was determined using the height difference

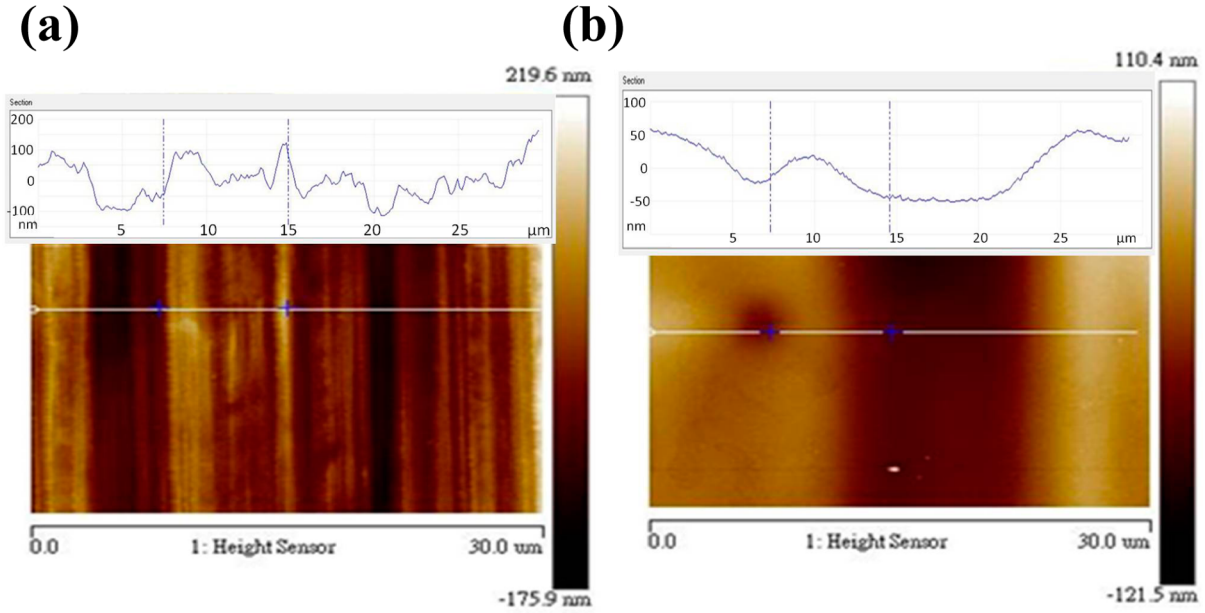

Figure 3. AFM images of (a) up-Cu and (b) p-Cu foils.

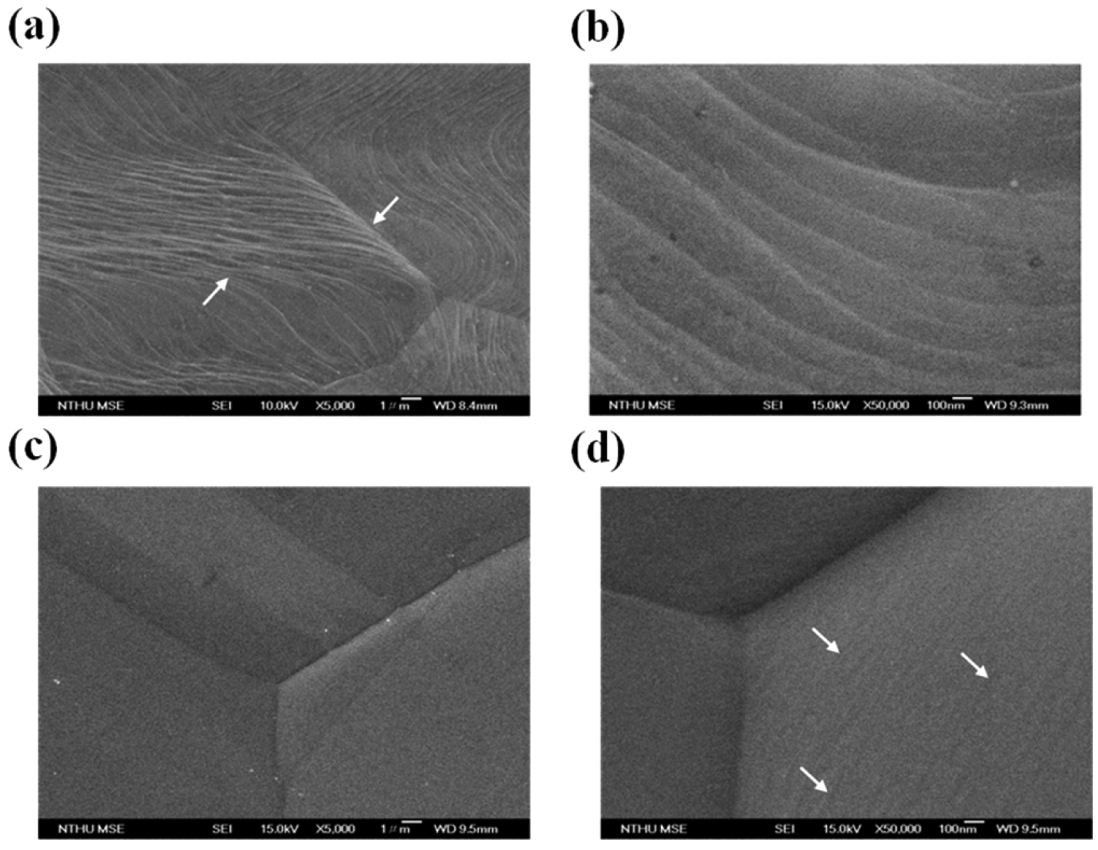

Figure 4. SEM images of graphene on the original Cu foil: (a) 5000×; (b) 50000×. SEM images of graphene on the p-Cu foil: (c) 5000×; (d) 50000×.

between graphene and the SiO_2/Si substrate, which is depicted in the upper part of Figure 2b. According to the thickness profile, we determined that the thickness of graphene was 0.7−1.0 nm, illustrating the thickness of the transferred graphene is thicker than that of the typical *d* spacing (0.337 nm) of graphite. This was most likely caused by the adsorption of water vapor or gas molecules on the graphene surface, which increases the graphene thickness. A broad range of thicknesses was reported when the AFM measurement was conducted in air, and a typical thickness in the range of 0.6−1.4 nm for single-layer graphene was suggested.[29,30] Both the 2D-band in the Raman spectrum and the thickness determined from AFM demonstrate the synthesis of high-quality single-layer graphene.

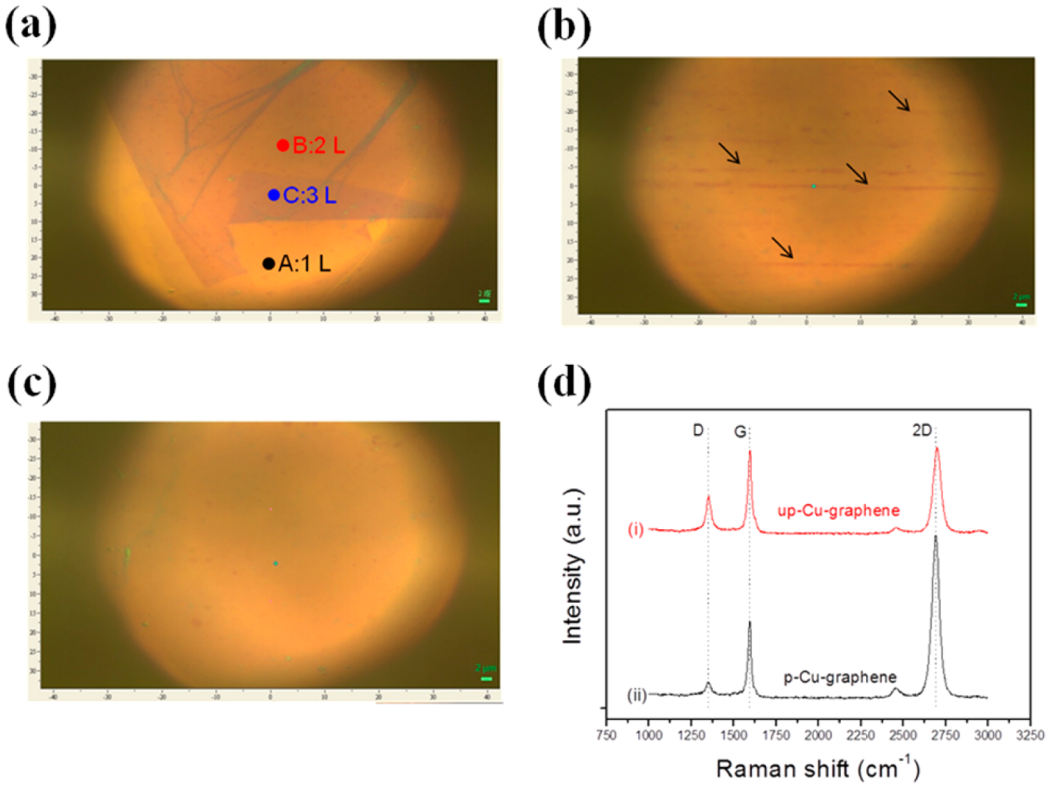

Figure 5. OM images of graphene on SiO_2/Si: (a) different numbers of graphene layers resulting in different colors; (b) graphene grown on the up-Cu foil; (c) graphene grown on the p-Cu foil. (d) Raman spectra of graphene on SiO_2/Si, where curve i shows the synthesis process in which the up-Cu foil was used, and curve ii shows the synthesis process in which the p-Cu foil was adopted.

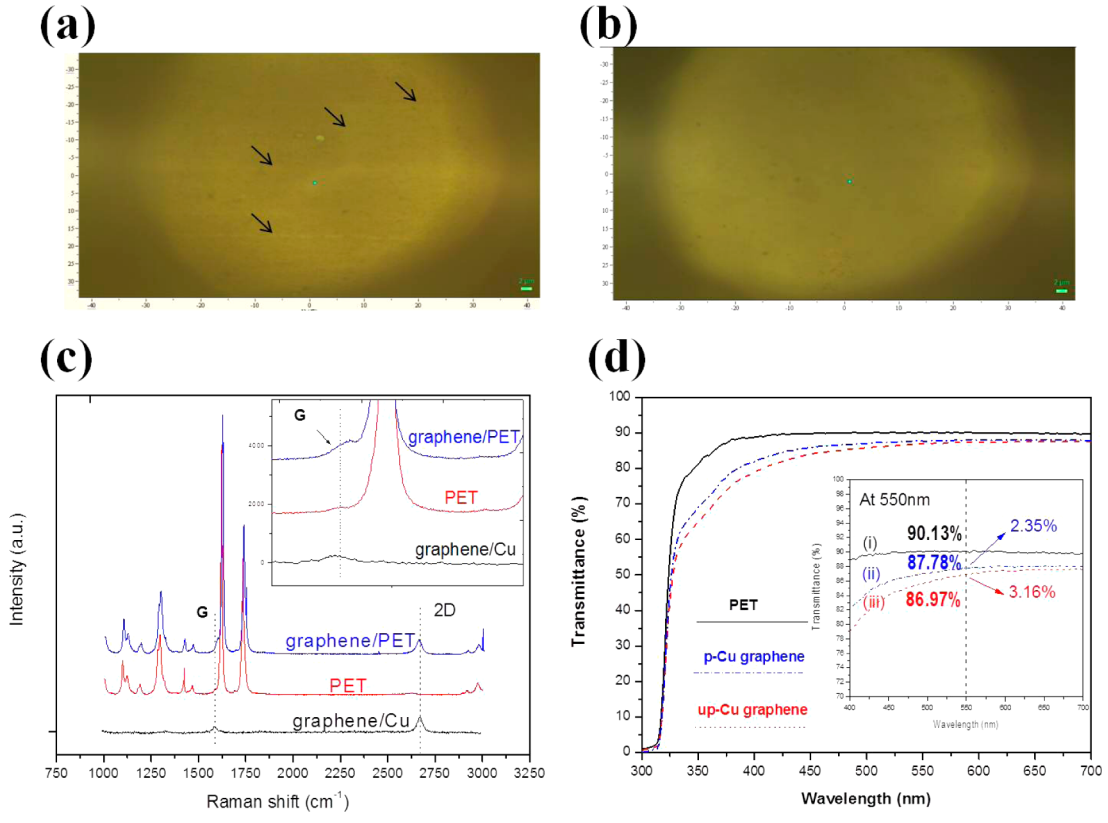

Figure 6. OM images of graphene on PET (a) using the up-Cu foil and (b) using the p-Cu foil. (c) Comparison of Raman spectra of graphene on p-Cu foil, PET, and graphene on PET. (d) Transmittance of PET (curve i), graphene (synthesized using p-Cu foil)/PET (curve ii), and graphene (synthesized using up-Cu foil)/PET (curve iii).

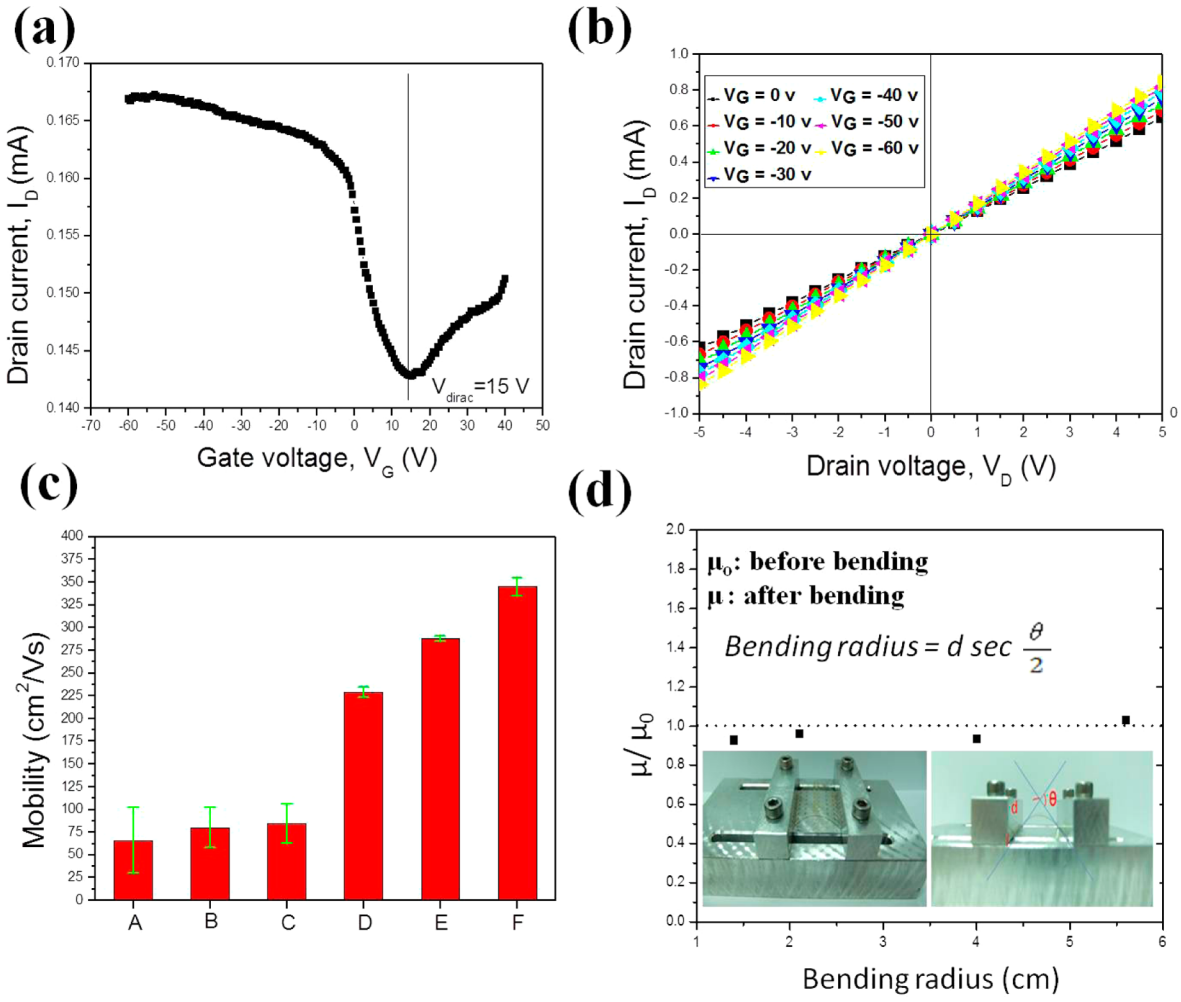

Figure 7. (a) Curve of the I_G–V_G and I_D–V_G (−60 to +40 V) relationships measured at V_D = 5 V. (b) I_D–V_D (−5 to +5 V) curve (V_G = 0, −10, −20, −30, −40, −50, and −60 V). Channel length: 10 μm. (c) Carrier mobility of six devices fabricated using various types of graphene. A–F represent devices labeled A–F. The number on the left side of the slash implies the channel length (μm), and the word on the right side of the slash indicates the substrates that did (yes) or did not (no) undergo electropolishing: (A) 10/no; (B) 15/no; (C) 20/no; (D) 10/yes; (E) 15/yes; (F) 20/yes (each datum represents the average of three experimental values). (d) μ/μ_0 versus bending radius. The inset on the lower left shows the bending instrument, and that on the lower right depicts the flexible transparent Gr-FET under bending.

In the electropolishing process, Cu foil (2.0 × 2.0 cm^2) was connected to the positive end of a power supply. AFM images of the up-Cu and p-Cu foils are shown in parts a and b of Figure 3, respectively. A rough surface containing undulating parallel hills and valleys with a roughness of 166 nm was detected, as shown in Figure 3a. Substantial improvement in the roughness with an R_{max} of 36 nm was achieved after electropolishing treatment was performed. The smooth surface of the Cu foil reduced the nucleation sites (grain boundaries and steps) for amorphous carbon deposition, consequently improving the graphene quality.

The SEM images indicate substantially different graphene topographies grown on the p-Cu and up-Cu foil substrates. On the surface of the up-Cu foil, grain boundaries, indicated by white arrows, and terrace-like morphology beneath the graphene are clearly observed, as shown in Figure 4a. Because of the highly uneven surface of the up-Cu foil, wrinkle-like graphene, depicted in Figure 4a,b, was clearly observed. Reconstruction of Cu atoms in the Cu foil at an elevated temperature caused the deposited graphene to be stressed and compressed, which produced wrinkle-like graphene. However, after the electropolishing and annealing processes were conducted, the grain size of the Cu foil was significantly increased and the roughness was considerably reduced. This promoted the reconstruction effect for obtaining smooth Cu foil, as a result alleviating the formation of wrinkle-like graphene, as shown in Figure 4c,d. The white arrows in Figure 4d indicate the smooth morphology of the as-deposited graphene on the Cu foil surface.

Because the as-purchased Cu foil has an extremely rough surface, the graphene deposited on the up-Cu foil exhibited considerable damage and numerous folded stripes, which were identical with the stripes on the undulating Cu foil when the PMMA film was dissolved in acetone. The p-Cu foil exhibited a smooth surface, resulting in the graphene film on the PET substrate displaying relatively little damage and fewer folded stripes.

The number of graphene layers can be estimated using OM by judging the color of the graphene on a 300 nm SiO_2/Si substrate.[31] Graphene exhibiting various colors marked at points A–C in Figure 5a indicates graphene with a monolayer, two layers, and three layers, respectively. Parts b and c of Figure 5 show the OM images of single-layer graphene on SiO_2/Si obtained using the up-Cu and p-Cu foil substrates for graphene

deposition, respectively. Numerous dark stripes, indicated by the arrows in Figure 5b, can be observed, and its corresponding Raman spectrum is illustrated by curve i in Figure 5d. I_D is high, and I_{2D}/I_G is approximately unity, which is attributed to the damaged and folded graphene in the darker stripe. On the other hand, graphene synthesized using the p-Cu foil exhibited a smooth surface without any darker folded stripes, as depicted in Figure 5c. The Raman spectrum shown in curve ii in Figure 5d shows evidence of improvement in the graphene quality, indicating that adopting p-Cu foil as a substrate can significantly enhance the graphene quality. A considerably low I_D peak accompanying a high I_{2D}/I_G ratio over 2.0 indicates that high-quality graphene can be maintained without severely damaging the microstructure, even after being transferred from Cu foil to a SiO_2/Si substrate.

Flexible transparent Gr-FETs were fabricated by transferring the as-synthesized graphene from Cu foil to PET. Parts a and b of Figure 6 show the OM images of single-layer graphene on PET, which was synthesized on the up-Cu and p-Cu foil substrates, respectively. In Figure 6a, several folded stripes, indicated by arrows, can be detected on graphene/PET, whereas smooth graphene on PET, depicted by the OM image in Figure 6b, indicates that using the p-Cu foil can produce high-quality graphene even after transfer. Raman spectra of graphene/Cu foil, PET, and graphene/PET are compared, as shown in Figure 6c. Characteristic peaks of PET in the Raman spectrum are considerably stronger than those of graphene; nevertheless, the G-band and 2D-band of graphene can be clearly observed in the Raman spectra. The inset in Figure 6c shows a small shoulder of the G-band in the graphene/PET curve, indicating the insignificant microstructure destruction of graphene, which demonstrates the successful transfer of high-quality graphene from p-Cu foil to the PET film. The transmittance of graphene/PET was measured using ultraviolet−visible spectroscopy, as shown in Figure 6d; curves i−iii indicate the transmittance of PET, graphene/PET (graphene synthesized using p-Cu foil), and graphene/PET (graphene synthesized using up-Cu foil), respectively. The theoretical transmittance and absorbance of single-layer graphene at a wavelength of 550 nm are 97.7% and 2.3%, respectively.[32] In this study, the transmittances of graphene/PET are 86.97% and 87.78% for graphene grown on the up-Cu and p-Cu foils, respectively, and the corresponding absorbances are 3.16% and 2.35%, respectively. The low transparency of graphene/PET shown in curve iii was attributed to the partial shielding of the emitting light by the folded graphene.

The drain current and gate voltage (I_D−V_G) relationship at V_D = 5.0 V was recorded by varying the gate voltages in the range from −60 to +40 V, as shown in Figure 7a. The drain current increased as the gate voltage varied from the Dirac point to negative voltage, indicating that the carrier transport mechanism of the Gr-FET device was mainly by the hole carriers. The bipolar I_D−V_G characteristic curve of the device was also clearly obtained, as shown in Figure 7a. The Dirac voltage (V_{dirac} = 15 V) offset in a positive direction indicates that the fabricated device was a p-type FET. Theoretically, V_{dirac} of a graphene-based FET should be zero for nondoped graphene; however, graphene films might absorb moisture in an atmospheric environment, and PR residue adhering to graphene during the photolithography process also caused the transistor to behave like a p-type FET.[33]

The relationships between the drain current and drain−source voltage (I_D−V_{DS}) swept from −5 to +5 V at gate voltages of 0, −10, −20, −30, −40, −50, and −60 V were measured on the Gr-FET with a channel length of 10 μm, as shown in Figure 7b, which illustrates the ohmic contacts between graphene and the metal electrodes. In addition, the carrier mobility of the Gr-FET with channel lengths of 10, 15, and 20 μm fabricated using p-Cu and up-Cu foils was measured. The carrier mobilities of the Gr-FETs were calculated based on eq 1. The carrier mobility of the Gr-FET using graphene synthesized from the p-Cu foil was 220−340 $cm^2/(V\ s)$, which was nearly 4 times higher than that of graphene prepared from the up-Cu foil [30−90 $cm^2/(V\ s)$], as shown in Figure 7c. Although the on/off ratio of the Gr-FET is between 1 and 2, the electropolishing process conducted on the Cu foil can significantly enhance the electronic transport property of the Gr-FETs. This was attributed to alleviation of the negative effects from defects and the folded structure while graphene was synthesized on the p-Cu foil. Variations in the carrier mobility of the Gr-FETs before and after bending were measured as shown in Figure 7d. Under bending, graphene subjected to stretching or compression may partially disintegrate the graphene structure and, consequently, deteriorate the electrical property. The bending test and radius measurement are shown in the inset of Figure 7d, where μ_0 and μ are the carrier mobility of the Gr-FETs before and after bending, respectively. The ratios of μ_0/μ shown in Figure 7d indicate that the mobility variation was limited when the flexible transparent FET was subjected to bending by changing the radius of curvature from 6.0 to 1.0 cm.

4. CONCLUSIONS

This study involved synthesizing homogeneous and high-quality single-layer graphene deposited on p-Cu foil by using a thermal CVD process. The high-quality graphene was used for fabricating flexible transparent Gr-FETs. We found that the roughness of the Cu foil affected the quality of the synthesized graphene and subsequently deteriorated the performance of the flexible transparent Gr-FETs. Gr-FETs with a carrier mobility of 340 $cm^2/(V\ s)$ were achieved when the p-Cu foil was used for graphene deposition, which was approximately 4 times higher than that of the Gr-FETs using the up-Cu foil for graphene preparation. p-type Gr-FETs were fabricated in this study, which might be caused by moisture absorption or the presence of adherent PR residue. In the bending tests, variations in μ/μ_0 were lower than 10% when the bending tests were performed by changing the radius of curvature from 6.0 to 1.0 cm, illustrating that graphene maintained its electrical properties under extreme bending conditions.

■ ASSOCIATED CONTENT

Supporting Information

Photograph and OM image of the flexible transparent Gr-FETs. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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